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Figure 1 is a schematic cross-sectional view of a semiconductor device. The device features a central channel region (1) and two gate regions (2A and 2B). The channel region is defined by a layer of material (3A) on top of a substrate (3B). The gate regions are defined by a layer of material (3B) on top of a substrate (3A). The channel region is also labeled with '10 中空領域' and '8 中空部'. The gate regions are labeled with '8 中電界' and '3a 開口'. The substrate is labeled with '2A' and '2B'. The channel region is also labeled with 'b1' and 'b2'.

<http://www19.ipdl.inpit.go.jp/PA1/result/detail/main/wAAAS4ayhIDA405161831P1.htm> 10/18/2010